Technical Reference

Tektronix

# P6960 and P6980
# High-density Logic Analyzer Probes with D-Max™ Probing Technology
# Design Guide

## 071-1521-00

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071152100

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# Design Guide

This design guide provides information for you to design a target-system board that accommodates the P69XX. The specifications and information in this design guide are preliminary and are subject to change. For more information, contact your Tektronix sales representative.

## Product Description

The P69XX logic analyzer probe family consists of two new connectorless compression probes with D-Max™ Probing Technology (shown in Figure 1) that are compatible with the TLA7AXX logic analyzer modules.

- P6960 — 34 channel single-ended data, differential clock with D-Max™ Probing Technology
- P6980 — 34 channel differential data and clock with D-Max™ Probing Technology

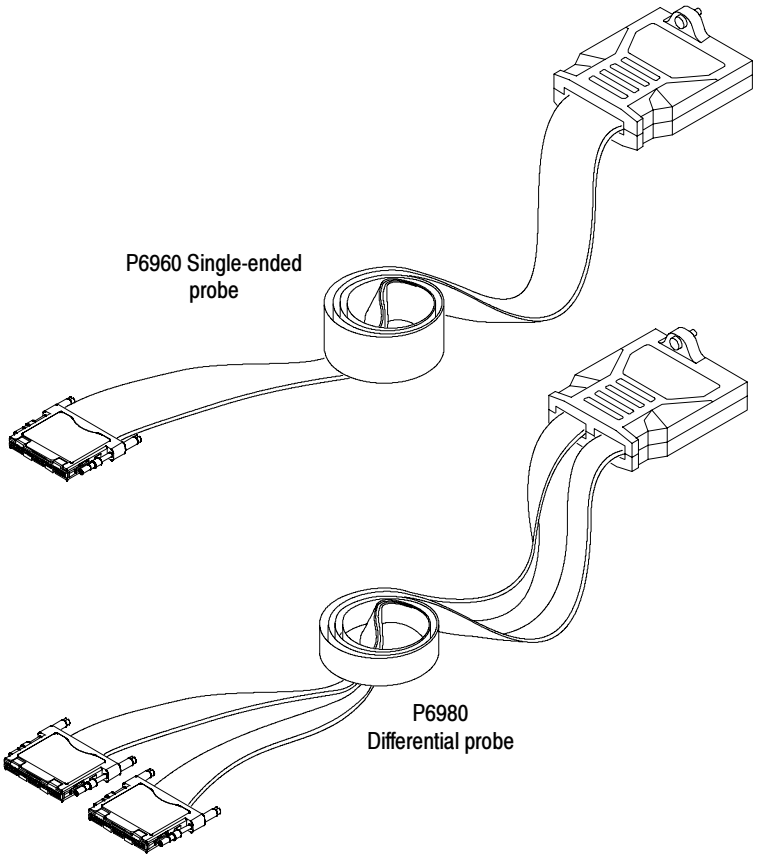
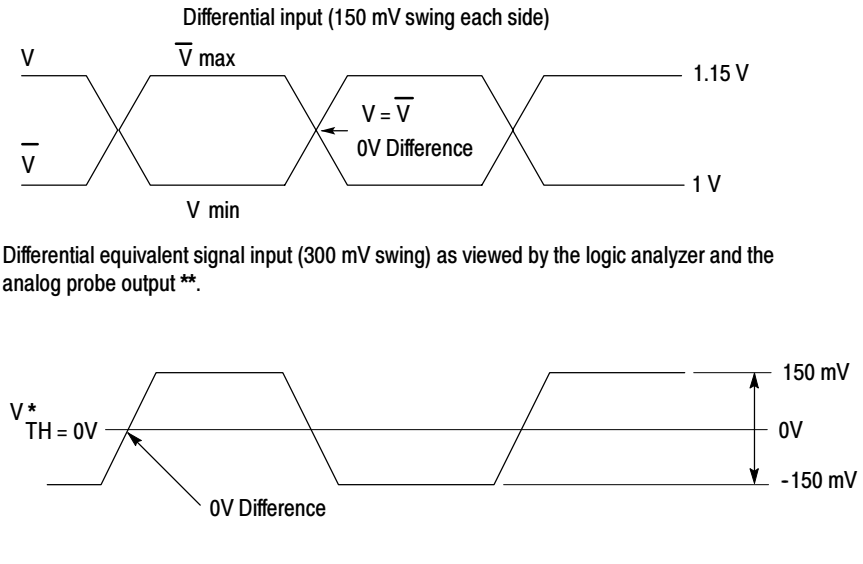



**Figure 1: P6960 and P6980 high-density probes**

### Differential Input Amplitude Definition

For differential signals, the magnitude of the difference voltage $\overline{V}$max-Vmin (and Vmin-$\overline{V}$max) must be greater than or equal to 150 mV. Refer to Figure 2.




*** For differential inputs, the module threshold should be set to 0V (assuming no common mode error).**

**** See online help for further analog output details.**

**Figure 2: Differential input amplitude**

Figure 3 shows the P69XX logic analyzer probe connected to a target system.

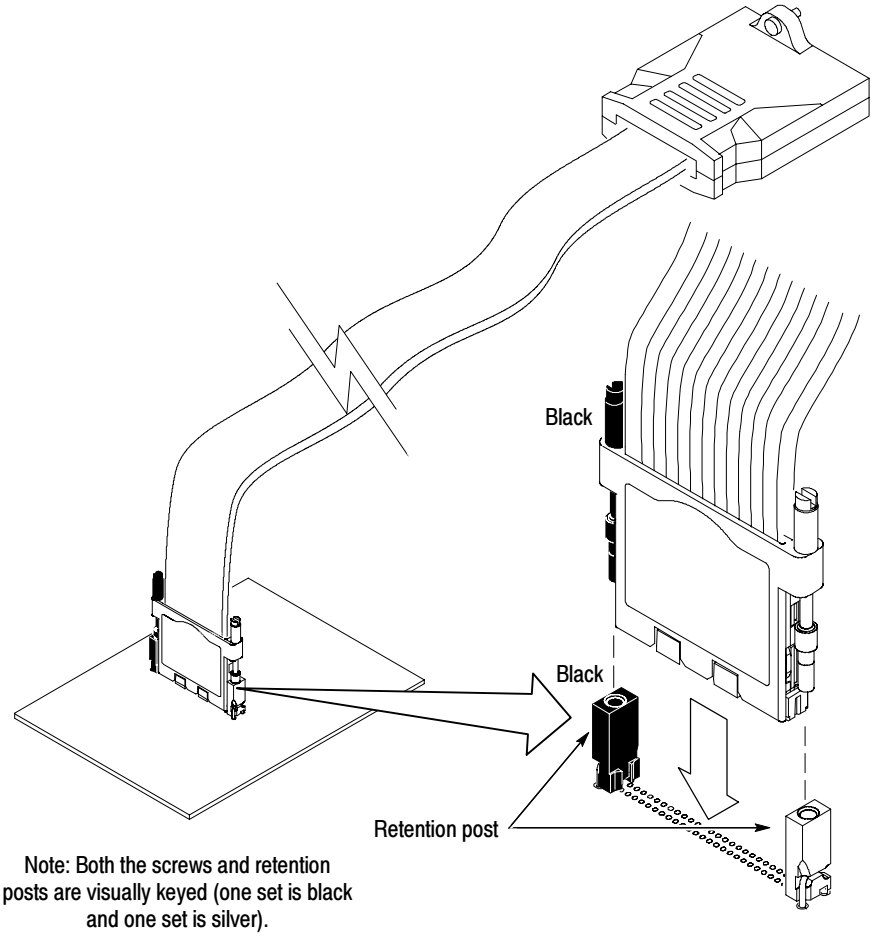



**Figure 3: P6960 single-ended probe connected to a target system**

# Board Design

This section provides information that helps you design your PCB mechanically and electrically for use with the P69XX logic analyzer probes.

## Probe Dimensions

Figure 4 shows the probe dimensions for the P6960 and P6980 probes.

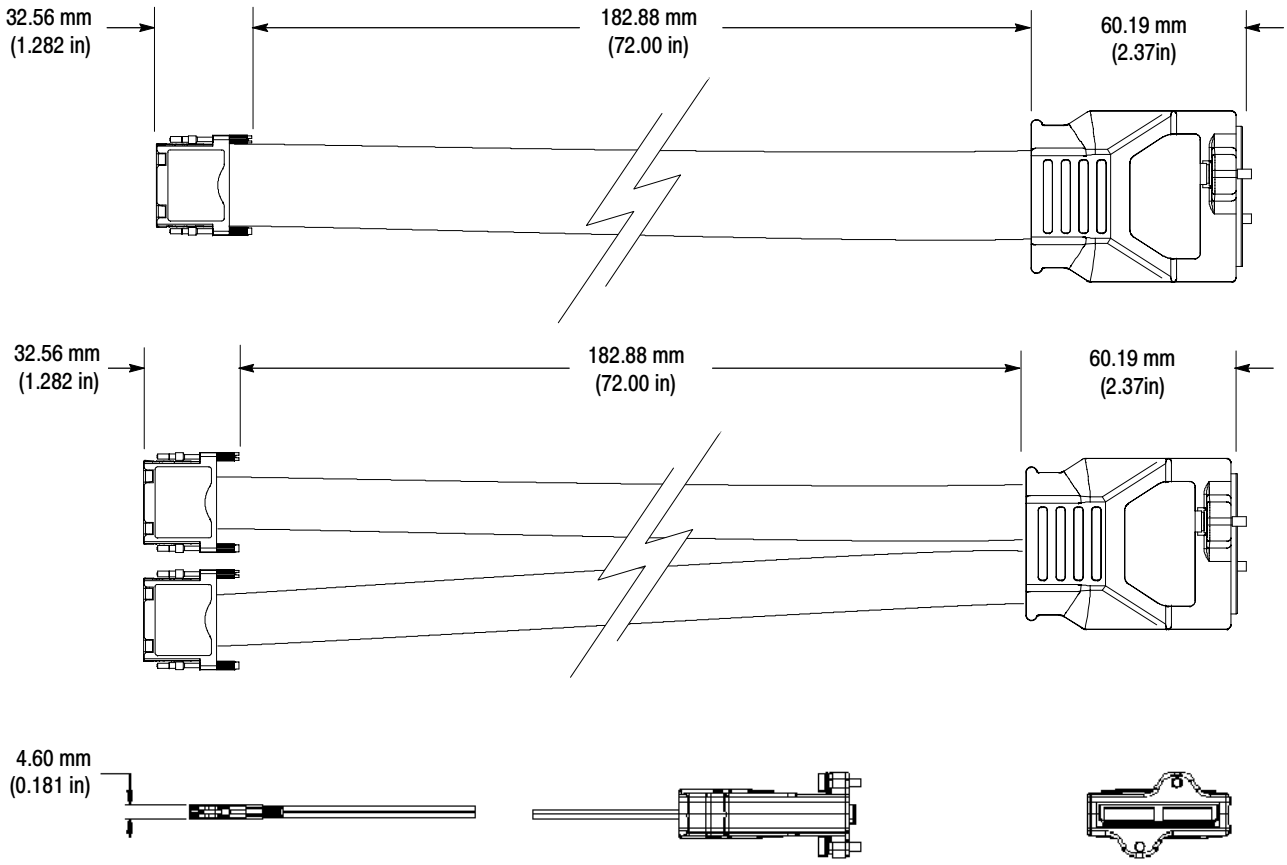



**Figure 4: P6960 and P6980 probe dimensions**

## Retention Post Dimensions and Keep out

The probes are attached to the PC board using two retention posts which ensures a reliable electrical and mechanical connection to your design, pin-to-pad alignment, and holds the probe securely to the board. Board thicknesses that are supported include 1.27 mm (0.050 in) to 6.35 mm (0.250 in).

***CAUTION.*** *To avoid solder creep, bend the post wires out after you insert the posts in the board, and then solder the post wires.*

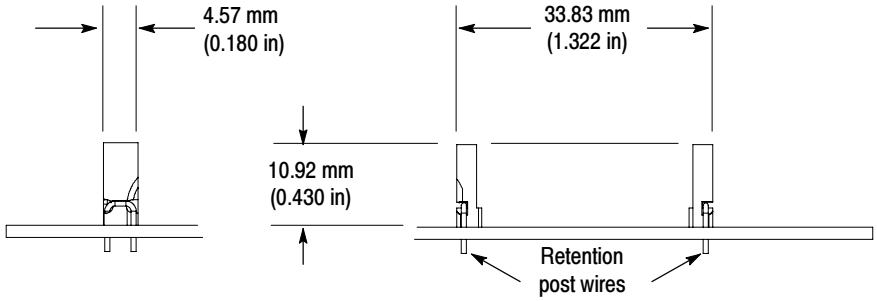



**Figure 5: Retention post dimensions**

Figure 6 shows the keep out area required for the retention posts. You must place vias, and route traces on the top layer of the board, outside of the keep out area.

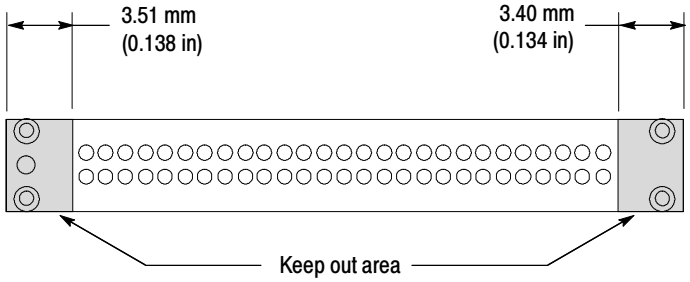



**Figure 6: Keep out area**

### Side-by-side and End-to-end Layout Dimensions

Figure 7 shows the dimensions for side-by-side footprint layout.

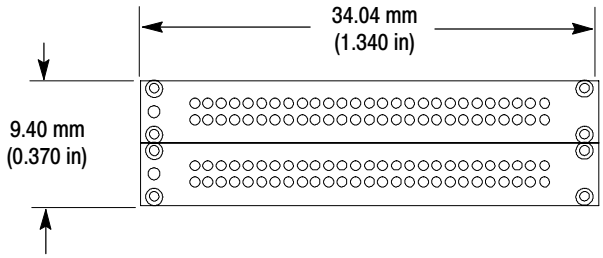



**Figure 7: Side-by-side layout**

Figure 8 shows the dimensions for an end-to-end footprint layout.

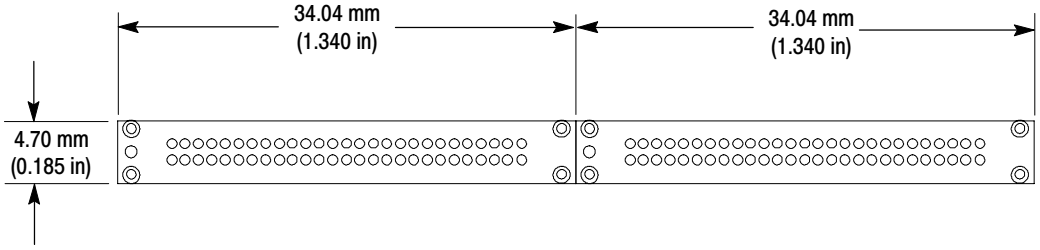



**Figure 8: End-to-end layout**

## Signal Routing

Figure 9 shows examples of pass through signal routing for a single-ended data configuration and a differential data configuration.

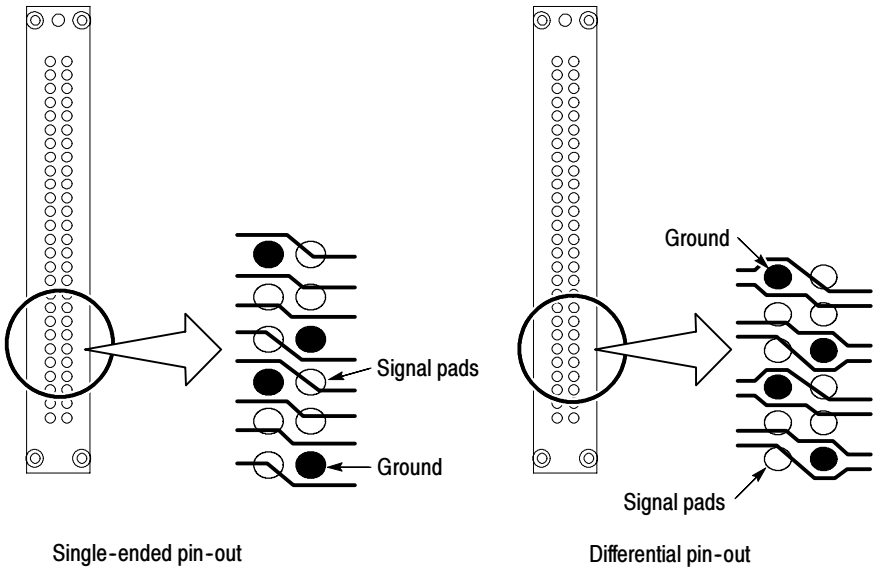



**Figure 9: Signal routing on the target system**

## Probe Footprint Dimensions

Use the probe footprint dimensions in Figure 10 to lay out your circuit board pads and holes for attaching the retention posts. Pad finishes that are supported include hot air solder level (HASL–see note), immersion silver, and immersion gold.

***NOTE**. Tektronix recommends using immersion gold surface finish for best performance. Test results show lower performance with HASL.*

*Tektronix also recommends that the probe attachment holes float or remain unconnected to a ground plane. This prevents overheating the ground plane and promotes quicker soldering of the retention posts to your PCB. The probe retention posts are designed to allow you to solder the retention posts from either side of your PCB.*

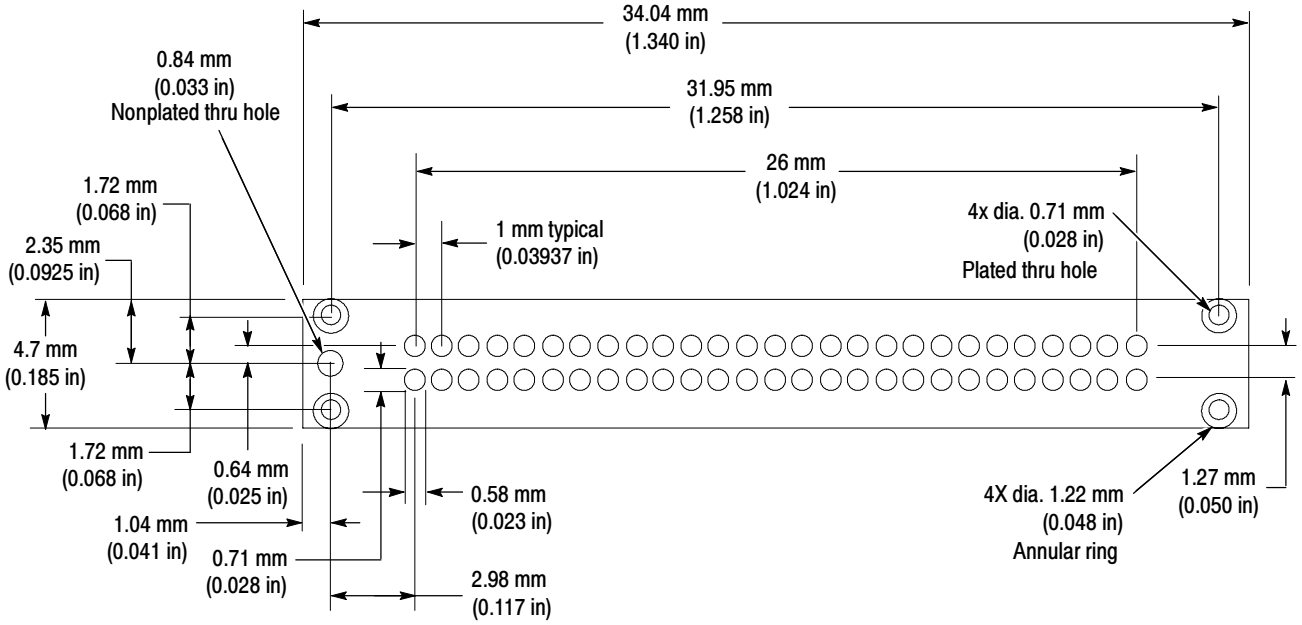



**Figure 10: Probe footprint dimensions**

***NOTE**. You must maintain a solder mask web between the pads when traces are routed between pads on the same layer. The solder mask must not encroach onto the pads within the pad dimensions shown in Figure 10.*

## Other Design Considerations

### Via-in-pad

Traditional layout techniques require vias to be located next to a pad and a signal routed to the pad, causing a stub and more PCB board area to be used for the connection. Many of today's new digital designs require you to minimize the electrical effects of the logic analyzer probing that you design into the circuit board. Using via-in-pad to route signals to the pads on the circuit board allows you to minimize the stub length of the signals on your board, thus providing the smallest intrusion to your signals. It also enables you to minimize the board area that is used for the probe footprint and maintain the best electrical performance of your design.

Figure 11 shows a footprint example where two pads use vias. Detail A describes the recommended position of the via with respect to the pad.

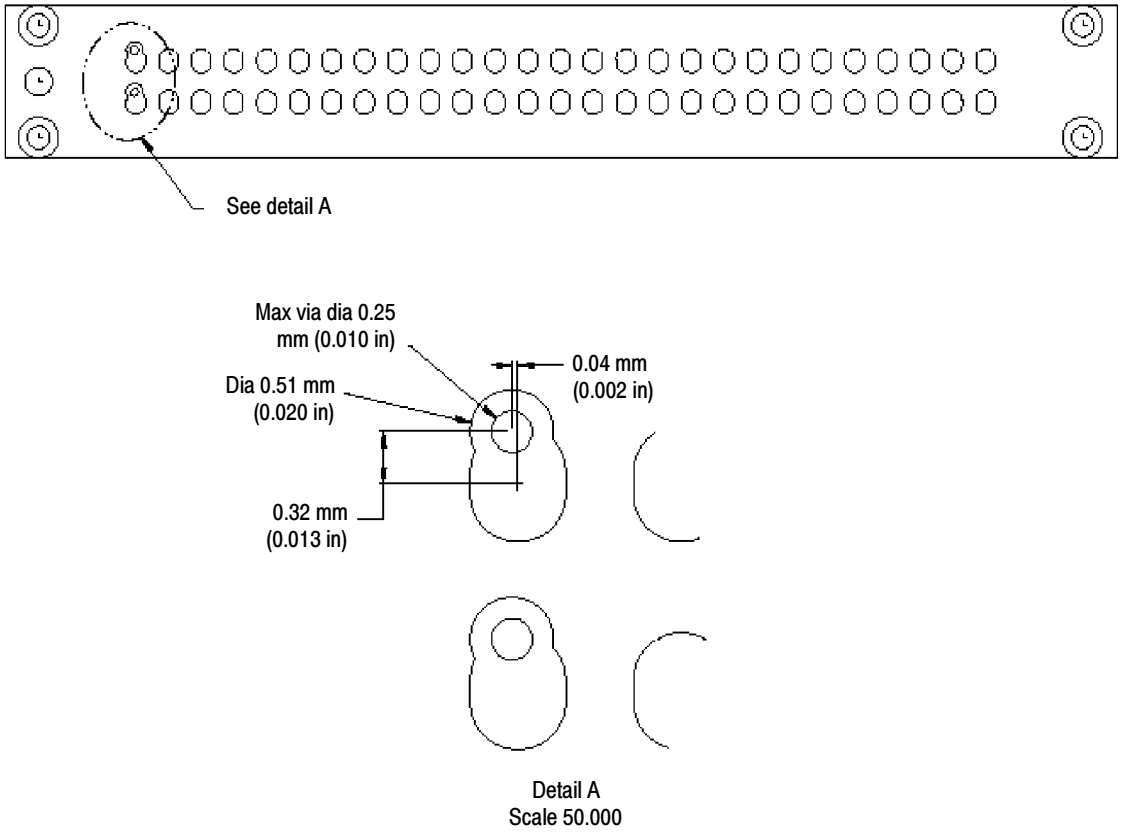



**Figure 11: Optional Via-in-Pad placement recommendation**

# Probe Pinout Definition and Channel Assignment

This section contains probe pinout definitions and channel assignment tables for P6960 and P6980 probes.

## P6960 Single-ended Probe with D-Max™ Probing Technology

Figure 12 shows the pad assignments, pad numbers, and signal names for the P6960 single-ended data, differential clock logic analyzer probe. The P6960 probe has 32 data channels, one clock, and one qualifier for each footprint.

Table 1 lists the channel mapping to a logic analyzer module for a P6960 single-ended data, differential clock logic analyzer probe.

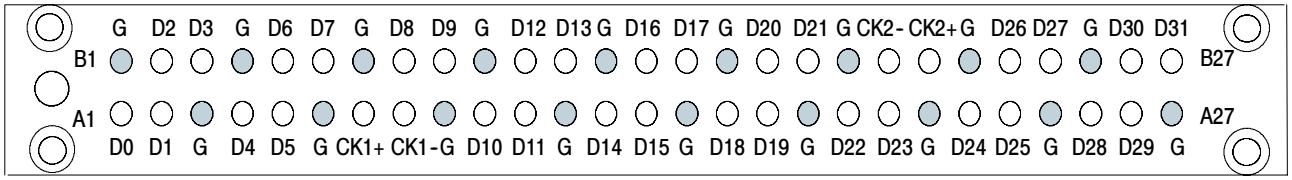



**Figure 12: P6960 single-ended pinout detail**

**Table 1: Channel assignment for a P6960 single-ended data, differential clock logic analyzer probe**

| | | 136 Channel | | | | 68 Channel | |
|---|---|---|---|---|---|---|---|
| | | | 102 Channel | | | | 34 Channel |
| Pin Number | Signal name | Probe4 | Probe 3 | Probe 2 | Probe 1 | Probe 2 | Probe 1 |
| A1 | D0 | E2:0 | A2:0 | A0:0 | C2:0 | A0:0 | C2:0 |
| A2 | D1 | E2:1 | A2:1 | A0:1 | C2:1 | A0:1 | C2:1 |
| A3 | GND | GND | GND | GND | GND | GND | GND |
| A4 | D4 | E2:4 | A2:4 | A0:4 | C2:4 | A0:4 | C2:4 |
| A5 | D5 | E2:5 | A2:5 | A0:5 | C2:5 | A0:5 | C2:5 |
| A6 | GND | GND | GND | GND | GND | GND | GND |
| A7 | CK1+ | Q3+ | CK0+ | CK1+ | CK3+ | CK1+ | CK3+ |
| A8 | CK1- | Q3- | CK0- | CK1- | CK3- | CK1- | CK3- |
| A9 | GND | GND | GND | GND | GND | GND | GND |
| A10 | D10 | E3:2 | A3:2 | A1:2 | C3:2 | A1:2 | C3:2 |
| A11 | D11 | E3:3 | A3:3 | A1:3 | C3:3 | A1:3 | C3:3 |
| A12 | GND | GND | GND | GND | GND | GND | GND |
| A13 | D14 | E3:6 | A3:6 | A1:6 | C3:6 | A1:6 | C3:6 |
| A14 | D15 | E3:7 | A3:7 | A1:7 | C3:7 | A1:7 | C3:7 |
| A15 | GND | GND | GND | GND | GND | GND | GND |

**Table 1: Channel assignment for a P6960 single-ended data, differential clock logic analyzer probe (Cont.)**

| | | 136 Channel | | | | 68 Channel | |
|---|---|---|---|---|---|---|---|
| | | | 102 Channel | | | | 34 Channel |
| Pin Number | Signal name | Probe4 | Probe 3 | Probe 2 | Probe 1 | Probe 2 | Probe 1 |
| A16 | D18 | E1:5 | D3:5 | D1:5 | C1:5 | D1:5 | A3:5 |
| A17 | D19 | E1:4 | D3:4 | D1:4 | C1:4 | D1:4 | A3:4 |
| A18 | GND | GND | GND | GND | GND | GND | GND |
| A19 | D22 | E1:1 | D3:1 | D1:1 | C1:1 | D1:1 | A3:1 |
| A20 | D23 | E1:0 | D3:0 | D1:0 | C1:0 | D1:0 | A3:0 |
| A21 | GND | GND | GND | GND | GND | GND | GND |
| A22 | D24 | E0:7 | D2:7 | D0:7 | C0:7 | D0:7 | A2:7 |
| A23 | D25 | E0:6 | D2:6 | D0:6 | C0:6 | D0:6 | A2:6 |
| A24 | GND | GND | GND | GND | GND | GND | GND |
| A25 | D28 | E0:3 | D2:3 | D0:3 | C0:3 | D0:3 | A2:3 |
| A26 | D29 | E0:2 | D2:2 | D0:2 | C0:2 | D0:2 | A2:2 |
| A27 | GND | GND | GND | GND | GND | GND | GND |
| | | | | | | | |
| B1 | GND | GND | GND | GND | GND | GND | GND |
| B2 | D2 | E2:2 | A2:2 | A0:2 | C2:2 | A0:2 | C2:2 |
| B3 | D3 | E2:3 | A2:3 | A0:3 | C2:3 | A0:3 | C2:3 |
| B4 | GND | GND | GND | GND | GND | GND | GND |
| B5 | D6 | E2:6 | A2:6 | A0:6 | C2:6 | A0:6 | C2:6 |
| B6 | D7 | E2:7 | A2:7 | A0:7 | C2:7 | A0:7 | C2:7 |
| B7 | GND | GND | GND | GND | GND | GND | GND |
| B8 | D8 | E3:0 | A3:0 | A1:0 | C3:0 | A1:0 | C3:0 |
| B9 | D9 | E3:1 | A3:1 | A1:1 | C3:1 | A1:1 | C3:1 |
| B10 | GND | GND | GND | GND | GND | GND | GND |
| B11 | D12 | E3:4 | A3:4 | A1:4 | C3:4 | A1:4 | C3:4 |
| B12 | D13 | E3:5 | A3:5 | A1:5 | C3:5 | A1:5 | C3:5 |
| B13 | GND | GND | GND | GND | GND | GND | GND |
| B14 | D16 | E1:7 | D3:7 | D1:7 | C1:7 | D1:7 | A3:7 |
| B15 | D17 | E1:6 | D3:6 | D1:6 | C1:6 | D1:6 | A3:6 |
| B16 | GND | GND | GND | GND | GND | GND | GND |
| B17 | D20 | E1:3 | D3:3 | D1:3 | C1:3 | D1:3 | A3:3 |
| B18 | D21 | E1:2 | D3:2 | D1:2 | C1:2 | D1:2 | A3:2 |
| B19 | GND | GND | GND | GND | GND | GND | GND |

**Table 1: Channel assignment for a P6960 single-ended data, differential clock logic analyzer probe (Cont.)**

| | | 136 Channel | | | | 68 Channel | |
|---|---|---|---|---|---|---|---|
| | | | 102 Channel | | | | 34 Channel |
| Pin Number | Signal name | Probe4 | Probe 3 | Probe 2 | Probe 1 | Probe 2 | Probe 1 |
| B20 | CK2- | Q2- | Q0- | CK2- | Q1- | CK2- | CK0- |
| B21 | CK2+ | Q2+ | Q0+ | CK2+ | Q1+ | CK2+ | CK0+ |
| B22 | GND | GND | GND | GND | GND | GND | GND |
| B23 | D26 | E0:5 | D2:5 | D0:5 | C0:5 | D0:5 | A2:5 |
| B24 | D27 | E0:4 | D2:4 | D0:4 | C0:4 | D0:4 | A2:4 |
| B25 | GND | GND | GND | GND | GND | GND | GND |
| B26 | D30 | E0:1 | D2:1 | D0:1 | C0:1 | D0:1 | A2:1 |
| B27 | D31 | E0:0 | D2:0 | D0:0 | C0:0 | D0:0 | A2:0 |

## P6980 Differential Probe with D-Max™ Probing Technology

Figure 13 shows the pad assignments, pad numbers, and signal names for the P6980 differential data and clock logic analyzer probe. The P6980 probe has 16 data channels, and one clock or qualifier for each footprint. There are two footprints associated with one P6980 probe.

Table 2 lists the channel mapping to a 136 channel or 102 channel logic analyzer module for the P6980 differential data and clock logic analyzer probe.

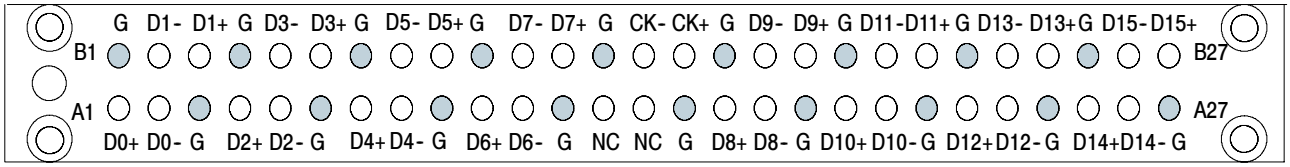



**Figure 13: P6980 differential pinout detail**

**Table 2: Channel assignment for a P6980 differential clock and data logic analyzer probe to a 136 or 102 channel logic analyzer module**

| | | 136 Channel | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | 102 Channel | | | | | |
| | | Probe 4 | | Probe 3 | | Probe 2 | | Probe 1 | |
| Pin number | Signal name | Head1 | Head2 | Head1 | Head2 | Head1 | Head2 | Head1 | Head2 |
| A1 | D0+ | E2:0+ | E0:0+ | A2:0+ | D2:0+ | A0:0+ | D0:0+ | C2:0+ | C0:0+ |
| A2 | D0- | E2:0- | E0:0- | A2:0- | D2:0- | A0:0- | D0:0- | C2:0- | C0:0- |

**Table 2: Channel assignment for a P6980 differential clock and data logic analyzer probe to a 136 or 102 channel logic analyzer module (Cont.)**

| | | 136 Channel | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | 102 Channel | | | | | |
| | | Probe 4 | | Probe 3 | | Probe 2 | | Probe 1 | |
| Pin number | Signal name | Head1 | Head2 | Head1 | Head2 | Head1 | Head2 | Head1 | Head2 |
| A3 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| A4 | D2+ | E2:2+ | E0:2+ | A2:2+ | D2:2+ | A0:2+ | D0:2+ | C2:2+ | C0:2+ |
| A5 | D2- | E2:2- | E0:2- | A2:2- | D2:2- | A0:2- | D0:2- | C2:2- | C0:2- |
| A6 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| A7 | D4+ | E2:4+ | E0:4+ | A2:4+ | D2:4+ | A0:4+ | D0:4+ | C2:4+ | C0:4+ |
| A8 | D4- | E2:4- | E0:4- | A2:4- | D2:4- | A0:4- | D0:4- | C2:4- | C0:4- |
| A9 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| A10 | D6+ | E2:6+ | E0:6+ | A2:6+ | D2:6+ | A0:6+ | D0:6+ | C2:6+ | C0:6+ |
| A11 | D6- | E2:6- | E0:6- | A2:6- | D2:6- | A0:6- | D0:6- | C2:6- | C0:6- |
| A12 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| A13 | NC | NC | NC | NC | NC | NC | ND | NC | NC |
| A14 | NC | NC | NC | NC | NC | NC | ND | NC | NC |
| A15 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| A16 | D8+ | E3:0+ | E1:0+ | A3:0+ | D3:0+ | A1:0+ | D1:0+ | C3:0+ | C1:0+ |
| A17 | D8- | E3:0- | E1:0- | A3:0- | D3:0- | A1:0- | D1:0- | C3:0- | C1:0- |
| A18 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| A19 | D10+ | E3:2+ | E1:2+ | A3:2+ | D3:2+ | A1:2+ | D1:2+ | C3:2+ | C1:2+ |
| A20 | D10- | E3:2- | E1:2- | A3:2- | D3:2- | A1:2- | D1:2- | C3:2- | C1:2- |
| A21 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| A22 | D12+ | E3:4+ | E1:4+ | A3:4+ | D3:4+ | A1:4+ | D1:4+ | C3:4+ | C1:4+ |
| A23 | D12- | E3:4- | E1:4- | A3:4- | D3:4- | A1:4- | D1:4- | C3:4- | C1:4- |
| A24 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| A25 | D14+ | E3:6+ | E1:6+ | A3:6+ | D3:6+ | A1:6+ | D1:6+ | C3:6+ | C1:6+ |
| A26 | D14- | E3:6- | E1:6- | A3:6- | D3:6- | A1:6- | D1:6- | C3:6- | C1:6- |
| A27 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| | | | | | | | | | |
| B1 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| B2 | D1- | E2:1- | E0:1- | A2:1- | D2:1- | A0:1- | D0:1- | C2:1- | C0:1- |
| B3 | D1+ | E2:1+ | E0:1+ | A2:1+ | D2:1+ | A0:1+ | D0:1+ | C2:1+ | C0:1+ |
| B4 | GND | GND | GND | GND | GND | GND | GND | GND | GND |

**Table 2: Channel assignment for a P6980 differential clock and data logic analyzer probe to a 136 or 102 channel logic analyzer module (Cont.)**

| | | 136 Channel | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | 102 Channel | | | | | |
| | | Probe 4 | | Probe 3 | | Probe 2 | | Probe 1 | |
| Pin number | Signal name | Head1 | Head2 | Head1 | Head2 | Head1 | Head2 | Head1 | Head2 |
| B5 | D3- | E2:3- | E0:3- | A2:3- | D2:3- | A0:3- | D0:3- | C2:3- | C0:3- |
| B6 | D3+ | E2:3+ | E0:3+ | A2:3+ | D2:3+ | A0:3+ | D0:3+ | C2:3+ | C0:3+ |
| B7 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| B8 | D5- | E2:5- | E0:5- | A2:5- | D2:5- | A0:5- | D0:5- | C2:5- | C0:5- |
| B9 | D5+ | E2:5+ | E0:5+ | A2:5+ | D2:5+ | A0:5+ | D0:5+ | C2:5+ | C0:5+ |
| B10 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| B11 | D7- | E2:7- | E0:7- | A2:7- | D2:7- | A0:7- | D0:7- | C2:7- | C0:7- |
| B12 | D7+ | E2:7+ | E0:7+ | A2:7+ | D2:7+ | A0:7+ | D0:7+ | C2:7+ | C0:7+ |
| B13 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| B14 | CK- | Q3- | Q2- | CK0- | Q0- | CK1- | CK2- | CK3- | Q1- |
| B15 | CK+ | Q3+ | Q2+ | CK0+ | Q0+ | CK1+ | CK2+ | CK3+ | Q1+ |
| B16 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| B17 | D9- | E3:1- | E1:1- | A3:1- | D3:1- | A1:1- | D1:1- | C3:1- | C1:1- |
| B18 | D9+ | E3:1+ | E1:1+ | A3:1+ | D3:1+ | A1:1+ | D1:1+ | C3:1+ | C1:1+ |
| B19 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| B20 | D11- | E3:3- | E1:3- | A3:3- | D3:3- | A1:3- | D1:3- | C3:3- | C1:3- |
| B21 | D11+ | E3:3+ | E1:3+ | A3:3+ | D3:3+ | A1:3+ | D1:3+ | C3:3+ | C1:3+ |
| B22 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| B23 | D13- | E3:5- | E1:5- | A3:5- | D3:5- | A1:5- | D1:5- | C3:5- | C1:5- |
| B24 | D13+ | E3:5+ | E1:5+ | A3:5+ | D3:5+ | A1:5+ | D1:5+ | C3:5+ | C1:5+ |
| B25 | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| B26 | D15- | E3:7- | E1:7- | A3:7- | D3:7- | A1:7- | D1:7- | C3:7- | C1:7- |
| B27 | D15+ | E3:7+ | E1:7+ | A3:7+ | D3:7+ | A1:7+ | D1:7+ | C3:7+ | C1:7+ |

Table 3 lists the channel mapping to a 68 channel or 34 channel logic analyzer module for the P6980 differential data and clock logic analyzer probe.

**Table 3: Channel assignment for a P6980 differential clock and data logic analyzer probe to a 68 or 34 channel logic analyzer module**

| | | 68 Channel | | | |
|---|---|---|---|---|---|
| | | | | 34 Channel | |
| | | Probe 2 | | Probe 1 | |
| Pin number | Signal name | Head1 | Head2 | Head1 | Head2 |
| A1 | D0+ | A0:0+ | D0:0+ | C2:0+ | A2:0+ |
| A2 | D0- | A0:0- | D0:0- | C2:0- | A2:0- |
| A3 | GND | GND | GND | GND | GND |
| A4 | D2+ | A0:2+ | D0:2+ | C2:2+ | A2:2+ |
| A5 | D2- | A0:2- | D0:2- | C2:2- | A2:2- |
| A6 | GND | GND | GND | GND | GND |
| A7 | D4+ | A0:4+ | D0:4+ | C2:4+ | A2:4+ |
| A8 | D4- | A0:4- | D0:4- | C2:4- | A2:4- |
| A9 | GND | GND | GND | GND | GND |
| A10 | D6+ | A0:6+ | D0:6+ | C2:6+ | A2:6+ |
| A11 | D6- | A0:6- | D0:6- | C2:6- | A2:6- |
| A12 | GND | GND | GND | GND | GND |
| A13 | NC | NC | ND | NC | NC |
| A14 | NC | NC | ND | NC | NC |
| A15 | GND | GND | GND | GND | GND |
| A16 | D8+ | A1:0+ | D1:0+ | C3:0+ | A3:0+ |
| A17 | D8- | A1:0- | D1:0- | C3:0- | A3:0- |
| A18 | GND | GND | GND | GND | GND |
| A19 | D10+ | A1:2+ | D1:2+ | C3:2+ | A3:2+ |
| A20 | D10- | A1:2- | D1:2- | C3:2- | A3:2- |
| A21 | GND | GND | GND | GND | GND |
| A22 | D12+ | A1:4+ | D1:4+ | C3:4+ | A3:4+ |
| A23 | D12- | A1:4- | D1:4- | C3:4- | A3:4- |
| A24 | GND | GND | GND | GND | GND |
| A25 | D14+ | A1:6+ | D1:6+ | C3:6+ | A3:6+ |
| A26 | D14- | A1:6- | D1:6- | C3:6- | A3:6- |
| A27 | GND | GND | GND | GND | GND |

**Table 3: Channel assignment for a P6980 differential clock and data logic analyzer probe to a 68 or 34 channel logic analyzer module (Cont.)**

| | | 68 Channel | | | |
|---|---|---|---|---|---|
| | | | | 34 Channel | |
| | | Probe 2 | | Probe 1 | |
| Pin number | Signal name | Head1 | Head2 | Head1 | Head2 |
| | | | | | |
| B1 | GND | GND | GND | GND | GND |
| B2 | D1- | A0:1- | D0:1- | C2:1- | A2:1- |
| B3 | D1+ | A0:1+ | D0:1+ | C2:1+ | A2:1+ |
| B4 | GND | GND | GND | GND | GND |
| B5 | D3- | A0:3- | D0:3- | C2:3- | A2:3- |
| B6 | D3+ | A0:3+ | D0:3+ | C2:3+ | A2:3+ |
| B7 | GND | GND | GND | GND | GND |
| B8 | D5- | A0:5- | D0:5- | C2:5- | A2:5- |
| B9 | D5+ | A0:5+ | D0:5+ | C2:5+ | A2:5+ |
| B10 | GND | GND | GND | GND | GND |
| B11 | D7- | A0:7- | D0:7- | C2:7- | A2:7- |
| B12 | D7+ | A0:7+ | D0:7+ | C2:7+ | A2:7+ |
| B13 | GND | GND | GND | GND | GND |
| B14 | CK- | CK1- | CK2- | CK3- | CK0- |
| B15 | CK+ | CK1+ | CK2+ | CK3+ | CK0+ |
| B16 | GND | GND | GND | GND | GND |
| B17 | D9- | A1:1- | D1:1- | C3:1- | A3:1- |
| B18 | D9+ | A1:1+ | D1:1+ | C3:1+ | A3:1+ |
| B19 | GND | GND | GND | GND | GND |
| B20 | D11- | A1:3- | D1:3- | C3:3- | A3:3- |
| B21 | D11+ | A1:3+ | D1:3+ | C3:3+ | A3:3+ |
| B22 | GND | GND | GND | GND | GND |
| B23 | D13- | A1:5- | D1:5- | C3:5- | A3:5- |
| B24 | D13+ | A1:5+ | D1:5+ | C3:5+ | A3:5+ |
| B25 | GND | GND | GND | GND | GND |
| B26 | D15- | A1:7- | D1:7- | C3:7- | A3:7- |
| B27 | D15+ | A1:7+ | D1:7+ | C3:7+ | A3:7+ |

## Electrical Load Models

Figure 14 shows the high-frequency equivalent load-model circuit for the P69XX logic analyzer probes.

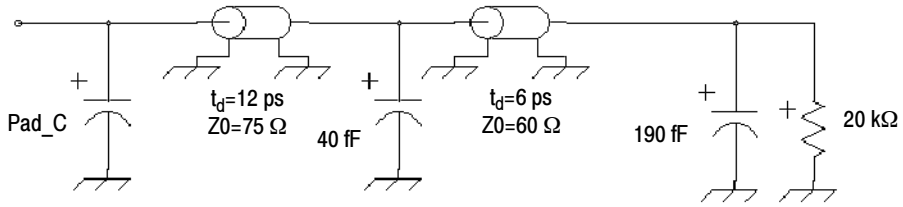



**Figure 14: P69XX high frequency load model**

Figure 15 shows the low-frequency equivalent load-model circuit for the P69XX logic analyzer probes.

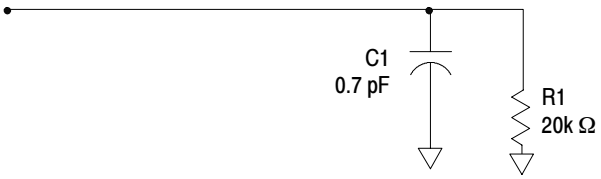



**Figure 15: P69XX low frequency load model**

## Legacy Probe and Attachment Support

- Nexus Technology, a Tektronix Partner, sells accessories that allow you to use the P6960 probe with legacy attachment connectors as well as utilize the P6960 probe footprint with select P68XX and P64XX probe products.
- Please contact Nexus Technology directly for more information.
- Contact Information:

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  Phone: 877-595-8116
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